Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **OUTPUT**
2. **ADJUST**
3. **INPUT**
4. **OUTPUT**
5. **OUTPUT**
6. **INPUT**

**.061”**

**3**

**4**

**5**

**6**

**1**

**2**

**EH1085**

**MASK**

**REF**

**.055”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: .005 X .005” min.**

**Backside Potential: OUTPUT**

**Mask Ref: EH1085**

**APPROVED BY: DK DIE SIZE .061” X .055” DATE: 3/1/22**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: SIS1085L-ADJ**

**DG 10.1.2**

#### Rev B, 7/19/02